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## REMARKS

Applicants appreciate the Examiner's thorough consideration provided the present application. Claims 1, 3-7 and 9-12 are now present in the application. Claim 7 has been amended. Claims 1 and 7 are independent. Reconsideration of this application is respectfully requested.

## Claim Rejections Under 35 U.S.C. §§ 102 & 103

Claims 1, 3, 4, 7, 9 and 10 stand under 35 U.S.C. § 102(b) as being anticipated by Yeo, U.S. Patent No. 6,521,939. Claims 5, 6, 11 and 12 stand rejected under 35 U.S.C. § 103(a) as being unpatentable Yeo. These rejections are respectfully traversed.

Independent claims 1 and 7 recite a combination of elements including "a bias voltage control terminal, coupled to said at least three n-type (for claim 1) /p-type (for claim 7) ion implant regions", "said first gate being disposed on a first side of said bias voltage control terminal" and "said second gate being disposed on a second side of said bias voltage control terminal opposite to said first side, said first gate and said second gate being disposed symmetrically to said bias voltage control terminal". Applicants respectfully submit that the above combination of elements as set forth in independent claims 1 and 7 is not disclosed nor suggested by the reference relied on by the Examiner.

Yeo discloses an integrated varactor on silicon. Although the Examiner alleged that Yeo in FIGs. 9-13 discloses all features of claim 1 and 7, Applicants respectfully disagree. As shown in FIG. 9 of Yeo, the left-side gate 108 and the right-side gate 108 are not disposed symmetrically to the metal layer 112 (referred to by the Examiner as the bias voltage control terminal of claims 1 and 7). In particular, the distance between the metal layer 112 and the left-side gate 108 is

larger than the distance between the metal layer 112 and the right-side gate 108, as shown in FIG.

9. Therefore, Yeo fails to teach "said first gate being disposed on a first side of said bias voltage

control terminal" and "said second gate being disposed on a second side of said bias voltage

control terminal opposite to said first side, said first gate and said second gate being disposed

symmetrically to said bias voltage control terminal" as recited in claims 1 and 7.

In addition, Yeo's metal layer 112 is patterned to form the interconnect lines and to

complete the manufacture of the IC device (see col. 6, lines 36-40), but cannot work as a bias

voltage control terminal for a differential variable capacitor. In particular, as shown in FIG 9 of

Yeo, the metal layer 112 is not coupled to the rightmost diffusion junction 104, which clearly

indicates that Yeo's metal layer 112 is not the "bias voltage control terminal, coupled to said at

least three n-type (for claim 1) /p-type (for claim 7) ion implant regions" as recited in claims 1

and 7.

To further clarify the present invention, Applicants respectfully submit that the present

invention provides for a symmetrical arrangement of the first and second gates to the bias

voltage control terminal to prevent the asymmetric interconnections of the differential capacitor.

By using Yeo's asymmetric structure of the left-side gate 108 and the right-side gate 108, the

inferior asymmetric interconnections of the differential capacitor will be inevitable, which is the

disadvantage the present invention has overcome.

The Examiner has correctly acknowledged that Yeo fails to disclose claims 5, 6, 11 and

12. However, the Examiner took his position that those features are commonly employed in the

art. Applicants respectfully traverse the Examiner position. If the Examiner persists in

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maintaining his position, Applicants respectfully request that the Examiner provide the reference(s) disclosing the features of claims 5, 6, 11 and 12 in the next Office Action.

Since Yeo fails to teach each and every limitation of independent claims 1 and 7 or their dependent claims, Applicants respectfully submit that claims 1 and 7 and their dependent claims clearly define over the teachings of Yeo. Accordingly, reconsideration and withdrawal of the rejections under 35 U.S.C. §§ 102 and 103 are respectfully requested.

## CONCLUSION

It is believed that a full and complete response has been made to the Office Action, and that as such, the Examiner is respectfully requested to send the application to Issue.

In the event there are any matters remaining in this application, the Examiner is invited to contact Joe McKinney Muncy, Registration No. 32,334 at (703) 205-8000 in the Washington, D.C. area.

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If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§1.16 or 1.17; particularly, extension of time fees.

Dated: December 21, 2005

Respectfully submitted,

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